REMARKS

Rejections under 35 USC §103(a)

Claims 1, 3 and 5 were rejected under 35 USC §103(a) as being unpatentable over Beilin et al. (U.S. Patent No. 5,916,453) in view of Albrecht et al. (U.S. Patent No. 4,968,585), and further in view of Ho et al. (U.S. Patent 5,354,712).

Maintaining the grounds of the previous rejection, the Examiner' added the allegation on the recitations "wherein a side face of each of said posts is covered by electrically conductive film so as to provide electrical contact between said one side and said other side of the substrate" as follows:

> Beilin and Albrecht do not specific disclose a side face of the post being covered by an electrically conductive film so as to provide electrical contact between said one side and other side of the substrate.
>
> Ho shows an interconnection structure as shown in figures 1a-1c comprising a side face of an inter connection (31) being covered by an electrically conductive film (22) so as to provide electrical contact between said one side and other side of a substrate (18).
>
> It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a side face of a post being covered by an electrically conductive film as taught by Ho employed in the substrate of Beilin and Albrecht in order to provide a protection barrier side surface for the post.

In Ho et al, reference numeral (31) indicates "copper contact areas"; reference numeral (22) indicates "steep side walls"; and reference numeral (18) indicates a dielectric layer. The Examiner apparently assumes that reference (24), which indicates a conformal layer of a conductive barrier material as the electrically conductive film rather than reference numeral (22) indicating side walls. According to Ho et al, the interconnection (31) made of copper is covered

by a conformal layer (24) made of a material titanium nitride, which is **less conductive** than copper.

Therefore, the disclosure of Ho et al provides no suggestion or motivation to cover a side face of each of the posts by electrically conductive film so as to provide electrical contact between said one side and said other side of the substrate.

Moreover, as discussed in the previous response, Beilin et al and Albrecht et al do not teach or suggest "A front-and-back electrically conductive substrate comprising: a plurality of posts extending through said substrate, said posts being anisotropically etched silicon, and each of the posts having an electrically conductive portion that has at least a first surface on one side of said substrate and a second surface on another side of said substrate; and an insulative substrate that supports the plurality of posts."

Beilin et al discloses methods of planarizing structures on wafers and substrates by polishing. Beilin et al describes in the relevant portion as follows:

> Referring to FIG. 14, photosensitive layer 112 is removed, and a new photosensitive layer 116 is formed over polish-stop layer 122 to form a composite layer comprising planarizing layer 120, polish-stop layer 122, and photosensitive layer 116. A plurality of apertures 117 are then formed through the composite layer. Apertures 117 are most readily formed by first pattern exposing photosensitive layer 116 to actinic radiation (for example UV light), developing layer 116, and then using layer 116 as an etch mask to transfer the pattern of apertures in layer 116 to layer 120 by a suitable etching process. An anisotropic etching process is preferred, such as for example plasma assisted etching processes. Reactive ion etching (RIE) is one preferred etching process. . . . .

(Col. 6, lines 7-18). Also, Beilin et al describes as follows:

> **Once apertures 117 are formed, they may be filled with material to form post 118 as shown in FIG. 15 with the deposition processes** described above with respect to the first generalized embodiment of the present invention. Thereafter, photosensitive layer 116 is removed, as shown in FIG. 16, and the resulting structure is polished, as shown in FIG. 17. . . . .

(Col. 6, lines 53-59). According to Beilin et al, the post 118 must be made by deposition processes. Nothing indicates that the post 118 can be made of anisotropically etched silicon.

Also, according to Beilin et al, the apertures are filled with conductive material, but the side face of the posts is NOT covered by electrically conductive film. Also, Albrecht et al does not discuss covering of the posts by electrically conductive film so as to provide electrical contact between one side and the other side of the substrate.

Albrecht et al discloses a microfabricated cantilever stylus with integrated conical tip. The abstract describes as follows:

> A cantilever stylus with an integrally formed conical tip is provided for atomic force microscopy AFM. The method for forming a stylus includes forming a circular masking pattern [14] on the surface of a silicon substrate and anisotropically etching the silicon to form a post [18] under the masking pattern. [See Figs2-3.] The post [18] is then isotropically etched to produce a conical silicon tip mold. [See Fig. 4.] In one embodiment of the invention the silicon substrate and the conical silicon tip mold are thermally oxidized to form a cantilever stylus having including a cantilever arm with a conical tip fixed to its free end. In another embodiment of the invention the silicon substrate and the conical silicon tip mold are coated with a thin film of a dielectric material to form a cantilever stylus with a conical tip. In this embodiment the backside of the stylus is coated with a conductive material and a strong electric field is applied to the tip to cause electromigration of the conductive material to the point of the tip.

(References to drawings added). The microfabricated cantilever stylus of Albrecht et al has nothing to do with the "posts being anisotropically etched silicon" recited in claim 1. Moreover, nothing in Albrecht et al indicates that the microfabricated cantilever stylus can be related to the front-and-back electrically conductive substrate as recited in claim 1.

There is no suggestion or motivation of combining the teaching of Albrecht et al with the teaching of Beilin et al. Moreover, Beilin et al and Albrecht et al do not teach or suggest "wherein a side face of each of said posts is covered by electrically conductive film so as to provide electrical contact between said one side and said other side of the substrate."

As pointed out in the previous response, the Examiner has not established a prima facie case of obviousness, which requires: (1) the prior art reference (or references when combined) must teach or suggest **all the claim limitations**; (2) there must be the **reason to attempt** (*PharmaStem Therapeutics, Inc. v. Viacell, Inc.* (Fed. Cir. July/2007)) to modify the reference or to combine reference teachings; (3) there must be a **reasonable expectation of success**. The rejection meets none of these requirements as discussed in the previous response.

In order to show the reason to attempt, a reference under 35 USC 103 must be analogous prior art. More specifically, in order to rely on a reference as a basis for rejection of an applicant's invention, the reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned. *In re Oetiker*, 977 F.2d 1443, 1446, 24 USPQ2d 1443, 1445 (Fed. Cir. 1992). See also *In re*

Deminski, 796 F.2d 436, 230 USPQ 313 (Fed. Cir. 1986); *In re Clay*, 966 F.2d 656, 659, 23 USPQ2d 1058, 1060-61 (Fed. Cir. 1992).

Here, the claimed invention is directed to a **front-and-back electrically conductive substrate**. On the other hand, Beilin et al discloses **method of planarizing** structures on wafers and substrates by polishing. Albrecht et al discloses a **microfabricated cantilever stylus** with integrated conical tip. These references are not in the field of applicant's endeavor or, reasonably pertinent to the particular problem with which the inventor was concerned.

Responding to Applicant's previous response, the Examiner alleged as follows:

> Examiner disagrees because the element (18 or 118) as disclosed in the Beilin reference deposit in the opening (117) by a CVD process and an **anisotropically etched process applied to remove a photoresist** (16 or 116) and layer (20 or 120) to formed post, so the technique as disclosed in the Beilin reference that **the posts (18 or 118) are formed by the anisotropicalliy etched process**.

(Office Action dated Aug. 8, 2006, page 5).

Claim 1, however, recites "said posts being anisotropically **etched silicon**" but NOT "said posts formed by anisotropically etched process." In Beilin et al, it is a photosensitive layer which is etched but not the pole. Moreover, the posts 18 or 118 are not silicon.

Regarding Albrecht et al, the Examiner alleged as follows:

> Examiner disagrees because as shown in figure 1 of Albrecht reference a silicon substrate (10) having top (12) and bottom surface (opposite surface of element 12), so **the silicon substrate is consider[ed] as a front and back electrically conductive substrate**. Further, the post (18) as disclosed, for example, in an abstract (see lines 4-6) clearly teaches that the post 18 is formed by anisotropically etched silicon.

(Office Action dated Aug. 8, 2006, page 6). The Examiner alleged that because the silicon substrate has top and bottom surfaces, the silicon substrate is considered as a front and back electrically conductive substrate. Here, the Examiner is merely applying the claimed term to the reference. The Examiner is taking advantage of knowledge other than what was within the level of ordinary skill in the art at the time the claimed invention was made. The knowledge is gleaned from applicant's disclosure. It is impermissible hindsight. The MPEP explains as follows:

> The requirement "at the time the invention was made" is to avoid impermissible hindsight. See MPEP § 2145, paragraph X.A. for a discussion of rebutting applicants' arguments that a rejection is based on hindsight.
>
> "It is difficult but necessary that the decisionmaker forget what he or she has been taught . . . about the claimed invention and cast the mind back to the time the invention was made (often as here many years), to occupy the mind of one skilled in the art who is presented only with the references, and who is normally guided by the then-accepted wisdom in the art." *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303, 313 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984).

(MPEP 2141.01(a) III). The Examiner further alleged:

> Thus, Beilin discloses the post that being formed by the anisotropically etched process, Albrecht teaches the post is formed by the anisotropically etched silicon. Therefore, it would have been obvious . . . to have a teaching of Albrecht employed in the substrate of Beilin in order to achieve a fine pitch interconnection in the wiring board.

However, the microfabricated cantilever stylus of Albrecht et al has nothing to do with the "posts being anisotropically etched silicon" recited in claim 1. Moreover, nothing in Albrecht et al indicates that the microfabricated cantilever stylus can be related to the front-and-back electrically conductive substrate as recited in claim 1. The Examiner does not

properly reason how the **method of planarizing** structures on wafers and substrates by polishing, disclosed in Beilin et al and the **microfabricated cantilever stylus** with integrated conical tip, disclosed in Albrecht et al are combined to result in the claimed **front-and-back electrically conductive substrate**.

For at least these reasons, claim 1 patentably distinguishes over Beilin et al, Albrecht et al and Ho et al. Claims 3 and 5, both directly depending from claim 1, also patentably distinguish over Beilin et al and Albrecht et al for at least the same reasons.

Claims 4 and 6 were rejected under 35 USC §103(a) as being unpatentable over Beilin et al. (U.S. Patent No. 5,916,453) in view of Albrecht et al. (U.S. Patent No. 4,968,585), and further in view of Onishi et al. (U.S. Patent 5,459,368)

Claims 4 and 6, all directly depending from claim 1, also patentably distinguish over Beilin et al and Albrecht et al for at least the same reasons.

Onishi et al was cited for allegedly disclosing an electronic device mounted on a pad of a substrate. Such disclosure, however, does not remedy the deficiencies of Beilin et al and Albrecht et al.

For at least these reasons, claims 4 and 6, patentably distinguish over Beilin et al, Albrecht et al and Onishi et al.

In view of the aforementioned amendments and accompanying remarks, Applicants submit that the claims, as herein amended, are in condition for allowance. Applicants request such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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